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Abstract	A buffer management device and method for improving buffer usage and access performance in a data processing system. A buffer device is located between two components in the data processing system and can be operated in the line mode and page mode. The buffer device typically comprises a number of memory blocks for temporarily storing the transmitted data, first tag memories, second tag memories and a mode-switching circuit. Each of the memory blocks includes a plurality of memory segments. In the line mode, the first tag memories store the addressing information and the memory blocks serve as the data storage unit. In the page mode, the second tag memories store the addressing information and the memory segments serve as the data storage unit. Therefore, data carried by different requests can be merged into the same memory block.		